ST. JOSEPH' COLLEGE (AUTONOMOUS), BANGALORE -27
MID SEMESTER TEST – AUGUST 2019
B.Sc. Electronics – V Semester
EL5215: Microprocessor and Interfacing

Time: 1 Hour **Max. Marks: 30**

Note: The question paper has three parts and one printed page.

PART A

Answer any three **03X5 = 15**

1. Draw internal architecture of Intel 8086 microprocessor and define BIU and EU.
2. Explain 1 MB memory organization for Intel 8086. How is the 20 bit Physical Address generated, explain with example.
3. Explain even and odd memory banking with an appropriate diagram,
4. Explain Interrupt Response Sequence with the help of a proper diagram.

PART B

Answer any three **03X4 = 12**

4. Draw and briefly discuss I/O write timing diagram for minimum mode configuration.
5. Write an ALP to find the average of ten given 8-bit numbers.
6. a. Write an ALP to divide a 16 bit number from and 8-bit number.

b. If **AX= D915H**; **BX = A1CFH** and **ADD AX, BX** is executed, what will be the status of **Carry**, **Auxillary Carry**, **Zero**, **Sign**, **Parity** and **Overflow** flags. Also write the 16bit flag register status after the operation, considering all other flags as RESET. (2+2)

7. Write an ALP to find the largest number from the series of 10 given 8- bit numbers.

PART C

Answer any three **03X1= 03**

7. Pipelining speeds up the process in Intel 8086 μP. Justify.
8. Write the addressing mode which the following instructions belong to:
i. Mov AX, 0005H
ii. Mov AX, [5000H]
iii. Mov AX, BX
iv. Mov AX,[BX]
9. State **true/false**:
i. The stack pointer register contains offset address of stack segment.
ii. Push operation decrements SP.
10. What is the difference between SUB (Subtract) and CMP (Compare) commands.