



**ST. JOSEPH’ S UNIVERSITY, BANGALORE - 27**

**OPEN ELECTIVE - 2 SEMESTER**

**ELOE 2.1 DIGITAL ELECTONICS FOR COMPUTERS**

**END SEMESTER EXAMINATION: MAY/JUNE 2023**

**Time: 90 min. Max. Marks: 60**

This question paper has **FOUR** printed pages.

**CHOOSE THE CORRECT ANSWER FROM THE OPTIONS GIVEN 60X01=60**

1. Way of representing numbers in 0's and 1's form is referred to as

a) binary notation b) decimal notation c) hexadecimal notation d) octal notation

2. Which number system is used for mathematical operations in Computers

a) Decimal b) Binary c) Octal d) Hexadecimal

3. Which gate has the output expression Y = M+N

a) OR gate b) AND gate c) NOT gate d) XOR gate

4. The symbol for two input AND gate is

a) b) c) d)

5. What is the weightage of LSB in decimal number system

a) 0 b) 10 c) 1 d) 100

6. The output expression of NAND gate with A and B input is

a) A+B b) (A+B)I c) (AB)I d) AB

7. A NOR gate followed by NOT gate will be resulting to

a) AND b) OR c) NAND d) XOR

8. The two inputs of a AND gate are A and 1, then the output is

a) A b) 1 c) 0 d) 1+ A

9. Gate that is also known as inverter is called

a) OR b) NOT c) XOR d) NAND

10. Gate whose output is 1 only when inputs are different is called

a) XOR b) XNOR c) NOR d) NAND

11. Gate having output 1 when either or all inputs are 1 is called

a) AND b) NOT c) OR d) NOR

12.Radix of binary number system is

a) 1 b) 2 c) 8 d) 10

13. In the given option which is not a basic gate

a) NAND b) OR c) AND d) NOT

14. Y = AI B + A BI is the output expression for

a) NOR b) XOR c) XNOR d) NAND

15. If the two inputs for AND gate are A and AI then the output is

a) A b) 0 c) 1 d) A

16. Which of the following expression is not for D Morgans theorem

a) A+B = B+A b) (A+B)I =AI BI c) (AB)I = AI + BI d) 

17. The logic circuit used to add three bits at a time is

a) Half adder b) Full adder c) Binary adder d) Parallel adder

18. In binary addition rules 1+1+1 is

a) 111 b) 10 c) 11 d) 01

19. In OR gate addition 1+A is

a) 0 b) A c) 1 d) AI

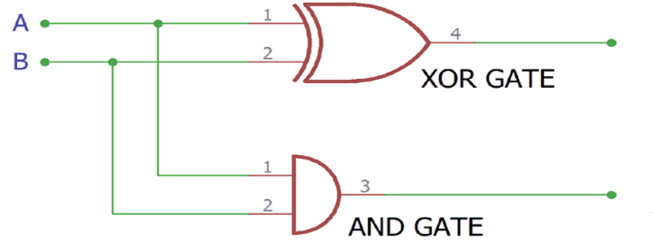
20. The two inputs for half subtractor is A=0 and B=1, then A minus B is

a) 1 b) 11 c) 10 d) 01

21.For a Half adder if A and B are the inputs then the expression for carry output is

a) A+B b) AB c) ABI d) (AB)I

22. The logic circuit given below is



a) Half adder b) Full adder c) Half subtractor d) Full subtractor

23. Total number of input terminals required for Full subtractor

a) 2 b) 3 c) 4 d) 1

24. How many control inputs are required for two input Multiplexer circuit

a) 3 b) 1 c) 2 d) 4

25. Which decimal number will be displayed when b and c segments are energized

a) 2 b) 1 c) 5 d) 7

26. How many output lines required for an ENCODER with 2N input lines

a) N b) N+1 c) N -1 d) 2N

27. If the number of gates in a IC less than ten, then it is named as

a) SSI b) LSI c) MSI d) ULSI

28. The fastest logic family is named as

a) TTL b) ECL c) CMOS d) DTL

29.The time taken by the gate to propagate a pulse from input to output is

a) Time period b) Propagation delay c) Average time d) Pulse time

30. The number of inputs that the gate is designed to handle is

a) Fan in b) Fan out c) Threshold d) Integration

31. The series of IC numbers used for military purpose starting with

a) 74 b) 72 c) 54 d) 94

32.The sequential circuit have \_\_\_\_\_\_\_\_\_\_\_\_ number of stable states

a) one b) two c) three d) four

33. In 74H series of logic family the letter H stands for

a) speed b) power c) noise d) propagation delay

34. The most important memory element is

a) Flip Flop b) Register c) Counter d) None of these

35. A flip flop known more formally as a

a) Mono stable b) Bistable c) Quasi stable d) None of these

36. A flip flop has ------ number of stable states

a) Two b) One c) Zero d) Four

37. The FF designed to overcome the disadvantage of RS flip flop

a) D b) JK c) T d) K

38. In a JK FF J = K = 1 is considered as

a) set b) reset c) toggle d) latch

39. The output of the sequential circuit depends upon

a) present input b) past input c) none of these d) present & past input

40. When the set is enabled in S-R flip flop then the output Q will be

a) 1 b) 0 c) no change d) indeterminate

41. The preset input is used to make output

a) Q= 1 b) Q=0 c) invalid d) no change

42. In a FF when preset = 0, clear =1 then the output will be

a) Q=1 b) Q=0 c) not used d) FF operation

43. The shift registers are categorized into

a) one b) two c) three d) four

44. What is the standard form of T flip flop

a) trigger b) toggle c) trigger &toggle d) none of these

45. \_\_\_\_\_\_\_\_ is an example for sequential circuit

a) Flip Flop b) Adder c) Decoder d) Multiplexer

46. The counters are categorized into \_\_\_\_\_\_

a) one b) two c) three d) four

47. How many states does the decimal counter have

a) four b) ten c) six d) nine

48. How many of states are there in a 4-bit counter

a) nine b) ten c) sixteen d) eight

49. Which IC is a decade counter

a) IC 7490 b) IC 7491 c) IC 7400 d) IC 7402

50. \_\_\_\_\_\_\_\_\_\_ type of counter counts in an upward manner

a) up counter b) down counter c) decade counter d) none of these

51. Memory location is a set of devices capable of storing one

a) bit b) byte c) pair d) word

52. Eight-bit microcomputer might consist of -------- latches

a) one b) eight c) two d) four

53. One byte is equal to

a) 4 bits b) 8 bits c) 2 bits d) 16 bits

54. In a memory device each latch stores ------ bit of word

a) one b) eight c) two d) four

55. In a memory device each location is referred to as a

a) latch b) address c) cell d) chip

56.The size of a memory is expressed as a

a) 2N b) 1010 c) 2N -1 d) 2N

57. If the size of the memory is 1024 it is abbreviated as

a) Kb b) Gb c) Mb d) Tb

58. In a binary address ranging from 00000 to 11111 ----- storage locations

a) 2 b) 32 c) 31 d) 5

59. In a binary address ranging from 00000 to 11111 need ---- of address inputs

a) 5 b) 32 c) 31 d) 2

60. A certain memory has a capacity of 8K×16 has ---- number of bytes

a) 8KBytes b) 16KBytes c) 16Bytes d) 8Bytes

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