

Register Number:

Date:

**ST. JOSEPH’ COLLEGE (AUTONOMOUS), BANGALORE - 27**

**SEMESTER EXAMINATION – APRIL 2019**

**B.Sc. Electronics – IV Semester**

**EL415: Verilog HDL**

**Time: 1 ½ hrs Max. Marks: 35**

Note: The question paper has three parts and one printed page.

**PART – A**

**Answer any THREE of the following 03X05=15**

1. What is a module? Discuss the four levels of design abstraction used in Verilog modeling.

2. Discuss the types of gate delays with proper example.

3. a. Write a note on concatenation operator and replication operator. **2+3**

b. Explain the difference between Regular delay control and intra assignment delay control with a proper example.

4. Write a note on parallel and sequential blocks used in behavioral modeling.

5. Write any five differences between tasks and functions.

**PART – B**

**Answer any THREE of the following 03X06=18**

6. a. Write a gate level design module for a 4 to 1 multiplexer.

b. Write a design (gate level) and test module to realize a 4 bit ripple carry adder. **2+4**

7. Write a design module (using case statement) and test module to realize a 1 to 4 demultiplexer.

8. Write a design module (behavioral modeling) and test module to realize a JK flip flop.

9. a. Write a module to design a clock with time period = 40 and duty cycle = 25%. Initial value of clock = 0.

b. Write a module using repeat loop to delay the statement a = a+1 by 20 positive edges of clock.

10. Write design and test module to realize a four bit ripple carry counter.

**PART – C**

**Answer any TWO of the following 02X01= 02**

11. Declare the following variables in Verilog: **2X0.5=1**

a. A memory MEM containing 256 words of 8 bit each.

b. A 16 bit storage register called address. Bit 15 must be MSB. Store the value of register to a bit decimal number equal to 10.

12. What is the advantage of connecting ports by names over connecting ports by ordered list?

13. If X= 8’b10101110; What will be stored in Y after the execution of the statement Y = X<<2;

14. Write expression for level sensitive timing control.

15. What is the use of generate block in Verilog.